www.YesLED.com / Info@YesLED.com

KYOCERA

MAR. 2019

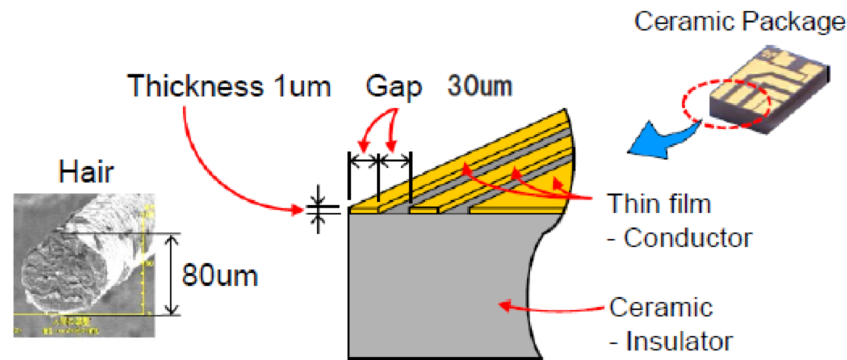
High Power Laser Submount Technical Introduction

"Thin Film Metallization"

Thin Film Deposition Available

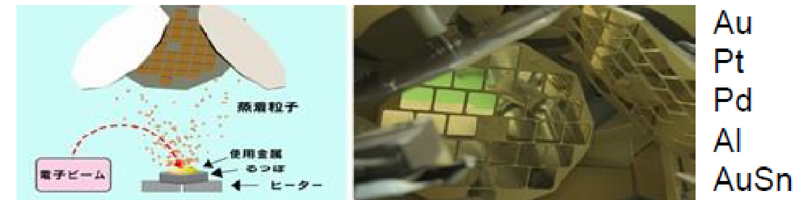
Thin film = A dense film having a thickness of a few microns to several tens of microns.
Based on the technique of forming thin metal as a conductor, a high density circuit is formed on the ceramic.
Metal : Cr, Cu, Ti, TiW, Pt, Pd, Au, SiO2, TaN2, NiCr, Al

➢ Overview



Line and Space of Thin film Metals are even finer than human hair

➢ Evaporation Method



Technology to deposit and deposit thermally evaporated particles

➢ Sputtering Method

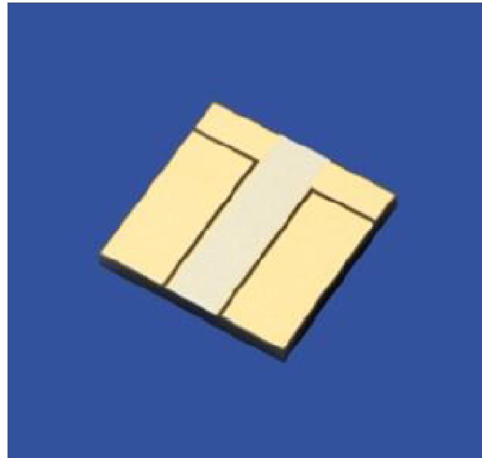
Technique of striking out particles by bombarding a metal target and depositing it

Pullback Free Submount for High-power Laser Diode

KYOCERA

Precise dicing and metallization technology enables to maximize the efficiency of uncooled high-power laser chip

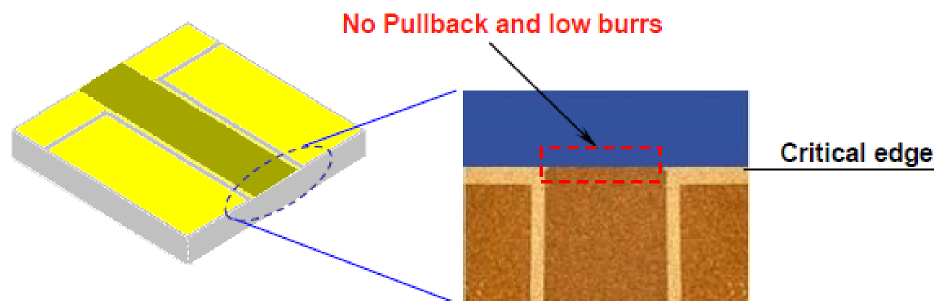
Product

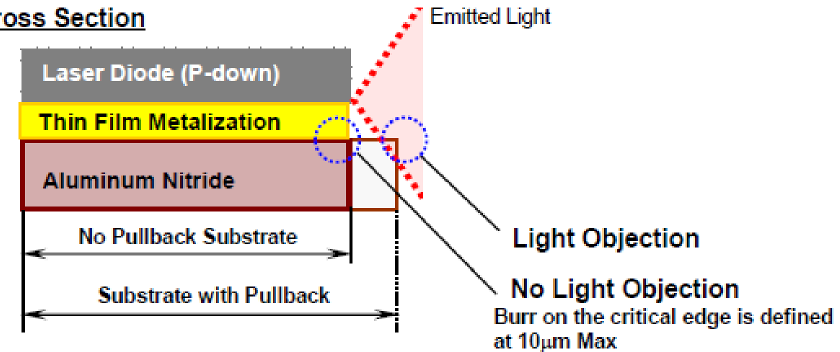


Features

- Light Obstruction Free Submount
  - No Pullback and Low Burrs（<10um) at Critical Edge
- Thin Film Metallization for pullback free
  - Ti-Pd-Au(5.0um)
- High 1st Level Reliability Material to Laser
  - C.T.E. : 4.6ppm/K @ R.T~400degC
- High Thermal Conductivity Material
  - 170W/mK Min. 200W/mK Min.
- Optimum AuSn for LD Chip Assembly
  - AuSn composition could be tuned according to the demand
- Serial Number Marking is Available
  - Enables Traceability to be controlled by serial number
- Precise Surface Condition
  - Flatness : 10 um Max. / Surface roughness 1.0um Max.

Structure

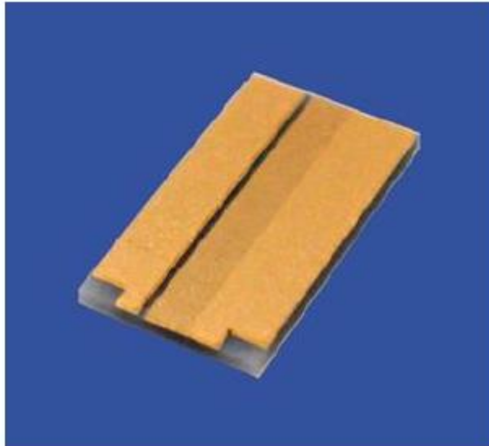




Thick Copper Plated Submount for High-power Laser Diode

Precise dicing and metallization technology enables to maximize the efficiency of uncooled high-power laser chip

Product

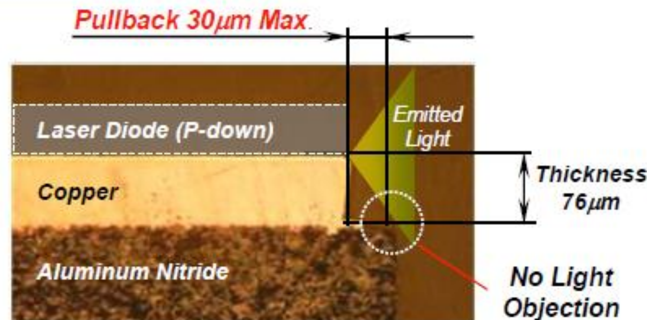


Features

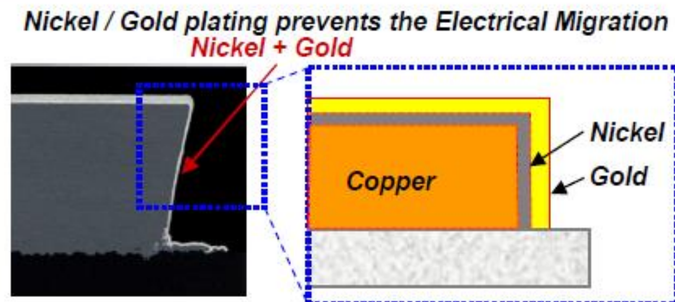
- Light Obstruction Free Submount
  - 30umMAX. Pullback at Critical Edge
- Thin Film Metallization for High-Current
  - Ti-Cu(76um)-Ni-Au
- Highly Reliable Plating
  - Ni-Au plating is formed to the side wall of copper
- High 1st Level Reliability Material to Laser
  - C.T.E. : 4.6ppm/K @ R.T~400degC
- High Thermal Conductivity Material
  - 170W/mK Min. 200W/mK Min.
- Optimum AuSn for LD Chip Assembly
  - AuSn composition could be tuned according to the demand
- Serial Number Marking is Available
  - Enables Traceability to be controlled by serial number
- Precise Surface Condition
  - Flatness : 10 um Max. / Surface roughness 1.0um Max.

Structure

Cross Section



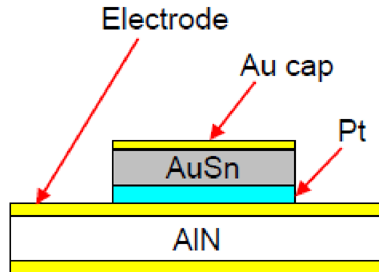
Highly Reliable Plating Structure



Thin Film AuSn for LD Chip Assembly

KYOCERA

Features



- AuSn deposition method : Evaporation
- Standard thickness : 3.0+/-0.5um (Customized thickness is available)
- AuSn is capped with the flash Au in order to avoid the oxidation.
- Barrier layer (Pt) exists under the AuSn
  The Pt layer is necessary for keeping the melting time of AuSn as long as possible.
  If barrier layer does not exist, Au underneath AuSn will come up then solve into AuSn.
  This makes Au rich condition to AuSn, then AuSn cannot keep the melting time.
- Standard composition ratio : Au(73+/5wt%)Sn (Customized composition ratio is available)
  If Au composition rate is higher, Dendrite will be likely to occur.

Observation Pt barrier

	Initial	After heating 320 deg C 30 sec
Ti-Pt-Au-AuSn	AuSn is diffused to electrode	
Ti-Pt-Au-Pt-AuSn	AuSn melting is Kept	

Observation AuSn composition

	Initial	After heating 320 deg C 60sec	After heating 320 deg C 210sec
Ti-Pt-Au-Pt-AuSn Au(70wt%)Sn	AuSn melting is Kept		
Ti-Pt-Au-Pt-AuSn Au(78wt%)Sn	Appeared the Dendrite to AuSn surface		

High Heat Dissipation Materials Line-up

KYOCERA

Material Line-up (High Heat Dissipation Materials Only)

New

	AN242 (Layer)	AN276 (Layer)	AIN170 (Single)	AIN200 (Single)	AN273 (Single)
Dielectric Constant (@1MHz)	8.7	8.8	9.0	8.7	8.8
Dielectric Loss Angle (x 10^{-4} @1MHz)	1.0	1.0	2.0	2.0	2.0
Volume Resistivity (W m @R.T.)	10^8	10^8	10^8	10^8	10^8
Thermal Conductivity (W/m K)	150 (min.)	170 (min.)	170 (min.)	190 (min.)	200 (min.)
Thermal Expansion (x 10^{-6} /K @40-400 °C)	4.7	4.8	4.6	4.6	4.5
Flexural Strength (MPa)	400	400	450	250	400

KYOCERA New Material can support higher thermal conductivity 200W/mK MIN.